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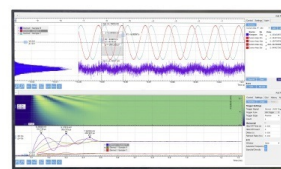
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ABSTRACT

We introduce a simplified fabrication technique for Josephson junctions and demonstrate superconducting Xmon qubits with T_1 relaxation times averaging above $50 \mu\text{s}$ ($Q > 1.5 \times 10^6$). Current shadow-evaporation techniques for aluminum-based Josephson junctions require a separate lithography step to deposit a patch that makes a galvanic, superconducting connection between the junction electrodes and the circuit wiring layer. The patch connection eliminates parasitic junctions, which otherwise contribute significantly to dielectric loss. In our patch-integrated cross-type junction technique, we use one lithography step and one vacuum cycle to evaporate both the junction electrodes and the patch. This eliminates a key bottleneck in manufacturing superconducting qubits by reducing the fabrication time and cost. In a study of more than 3600 junctions, we show an average resistance variation of 3.7% on a wafer that contains forty $0.5 \times 0.5\text{-cm}^2$ chips, with junction areas ranging between 0.01 and $0.16 \mu\text{m}^2$. The average on-chip spread in resistance is 2.7%, with 20 chips varying between 1.4% and 2%. For the junction sizes used for transmon qubits, we deduce a wafer-level transition-frequency variation of 1.7%–2.5%. We show that 60%–70% of this variation is attributed to junction-area fluctuations, while the rest is caused by tunnel-junction inhomogeneity. Such high frequency predictability is a requirement for scaling-up the number of qubits in a quantum computer.

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Superconducting quantum circuits constitute a promising architecture for the realization of quantum computers. Over the past two decades, many researchers have strived to improve the fabrication processes of superconducting circuits to increase the quantum-coherence time.^{1–3} On the other hand, the fabrication reproducibility has only recently gained considerable interest, motivated by the need for a scalable process to engineer multiqubit systems.^{4–11} Variation of the Josephson inductance represents the dominant cause of qubit-frequency variation, e.g., for the transmon-type qubit.¹² It is, therefore, important to increase the reproducibility of Josephson junctions (JJs) in order to enable pulsed-microwave control while avoiding crosstalk, a necessity for scaling up to tens of coupled qubits and more.^{13–15} Reproducibility is also important for various superconducting devices, particularly, the traveling-wave parametric amplifier (TWPA),^{16–21} which requires impedance matching and identical inductances along the long, lumped-element transmission line to avoid reflections and signal loss.

The most common material combination of JJs for qubit applications consists of an aluminum/aluminum oxide/aluminum (Al/ AlO_x /Al) sandwich fabricated by double-angle shadow evaporation of aluminum, within one vacuum cycle, with controlled *in situ* oxidation in between to form the tunneling barrier.^{22,23} Maintaining a galvanic, superconducting contact between the JJ's electrodes and the rest of the circuit is important, in order to avoid forming “parasitic” junctions in series, whose dielectric loss tangent contributes to decoherence and parameter fluctuations.^{1,24} In fact, in a recent study, Lisenfeld *et al.*²⁵ found that a major part of the two-level-system (TLS) defects responsible for dielectric loss may be located within the parasitic junction formed due to the shadow evaporation technique, with another significant contribution located at circuit interfaces, while the contribution of the small-size JJ itself can be negligible. Additionally, Nersisyan *et al.*² showed that the area of this parasitic junction adversely affects the coherence of the qubit. To mitigate this issue, the parasitic junction can be eliminated by depositing a patch (or bandage) layer that

connects the junction electrodes to the rest of the circuit, after removal of the native oxide of aluminum.²⁶ However, the further processing introduced by adding the patch can introduce more losses, especially those caused by interfacial resist residues that are difficult to remove.²⁷

In this work, we propose and demonstrate a technique to fabricate both the junction and the patch layer in a single lithography step by evaporating from three angles. We name the technique patch-integrated cross-type (PICT), with reference to the cross-type Josephson junctions first proposed by Potts *et al.*²³ We favorably evaluate the quality and reliability of our process by characterizing both the qubit coherence and the fabrication reproducibility. We measured the T_1 relaxation and T_2^* Ramsey free-induction decay times and their fluctuations, showing an average quality factor, $Q = 1.6 \times 10^6$, i.e., without additional losses in comparison to our standard fabrication process. ($Q = 2\pi f_{01} T_1$, where f_{01} is the qubit transition frequency.)²⁸ In addition, we characterized the reproducibility of the JJ parameters by fabricating a statistically significant number (>3600) of Josephson junctions and measuring their normal resistance, R_N , at room temperature. R_N is directly proportional to the Josephson inductance, L_J , and therefore, the measurement of R_N provides information on reproducibility of the qubit frequency, f_{01} .^{9,12,29} The measured inter-chip coefficient of variation (CV), the standard deviation divided by the mean, is 3.7% across a wafer, which drops to an average on-chip value of 2.7%. Furthermore, the resistance spread increases with decreasing junction size: for sizes used in fixed-frequency transmon qubits (0.02 – $0.06 \mu\text{m}^2$), we found a wafer-level variation of 3.4%–4.9%, corresponding to 1.7%–2.5% in qubit frequency.

The process described in this work builds on the background of our previous standard qubit design and fabrication techniques.²⁸ The layout of a typical device is shown in Fig. 1(a): it consists of a transmon/Xmon-type qubit^{12,30} (i) that is capacitively coupled to a readout resonator (ii), which is inductively coupled to a transmission line (iii). In our standard fabrication process,^{28,30} the aluminum ground plane is first deposited using electron beam evaporation. The wiring (transmission line, resonator, and shunt capacitor) and the flux trapping holes are then patterned using optical lithography and etched using wet chemistry. Figure 1(b) shows the JJ layout and the bandages or patches commonly used to connect it to the rest of the circuit.²⁶ The junction itself (A) is patterned using electron beam lithography (EBL), where proximity error correction (PEC) is used to optimize the dose factors for each junction based on its size. The Al layers are then deposited using the cross technique²³ (two thin-film depositions at an angle separated by a 90° planetary turn and oxidation to form the tunneling

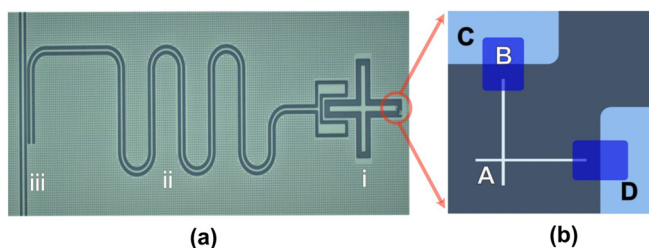


FIG. 1. (a) Micrograph of a device, consisting of an Xmon qubit (i) capacitively coupled to a resonator (ii), which is inductively coupled to a transmission line (iii). (b) Layout of the Josephson junction (A) and the patch for the standard process (B), connecting the junction electrodes to the Xmon capacitor (C) and ground (D).

barrier), in a Plassys MEB 550s evaporator, followed by liftoff. Next, the patch layer (B) is patterned in a final lithography step, which ensures galvanic connection of the junction to the capacitor (C) and the ground plane (D). After development, the oxide layer on top of the aluminum is ion-milled *in situ* before the deposition of the patch and liftoff.

In our PICT process, we pattern both the junction and the patch in one EBL step and evaporate the thin films within one vacuum cycle. A modification to the patch layout makes this possible, as shown in Fig. 2, where instead of rectangles, the patches are shaped like 45° fringes to provide selective deposition and milling when the resist is

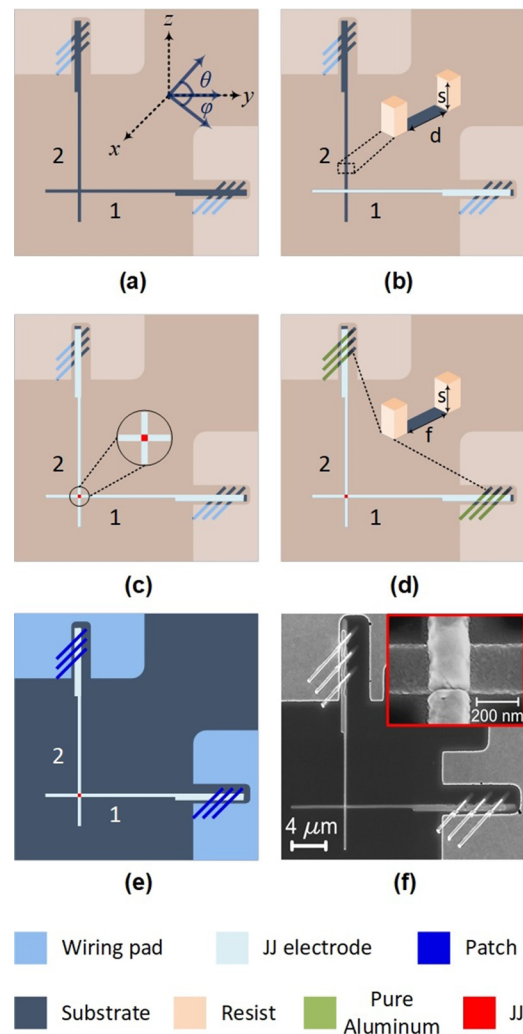


FIG. 2. (a)–(e) Schematic of the PICT process flow, showing the layout after (a) development, (b) deposition of the first electrode, (c) deposition of the second electrode, (d) ion milling of the aluminum oxide with the exposed, pure aluminum shown in green, and (e) patch deposition and resist removal. θ and φ are the planetary and tilt angles of the sample holder, respectively. Deposition of Al on top of the resist is not shown for clarity. (f) SEM image of the fabricated junction with the patch layer.

thick enough. This eliminates an entire lithography run and reduces the total steps of Josephson-junction fabrication by 50%.

The subsequent evaporation steps are shown in Figs. 2(a)–2(e), where θ and φ are the planetary and tilt angles (from the y-axis) of the sample holder, respectively. The evaporation and ion milling are both perpendicular to the yz-plane, pointing toward the $-x$ direction. The reference position is shown in Fig. 2(a), where $\varphi = \theta = 0^\circ$. When the angles are set at $\theta = \theta_1$ and $\varphi = \varphi_1$, first, the sample holder turns counterclockwise around the x-axis by θ_1 degrees in the yz-plane. Next, the sample holder turns (tilts) around the z-axis by φ_1 degrees.

The first junction electrode (1) is deposited at $\theta = 0^\circ$ and $\varphi = 45^\circ$ [Fig. 2(b)] and oxidized to form the tunneling barrier. The second electrode (2) is then deposited at $\theta = -90^\circ$ and $\varphi = 45^\circ$ in Fig. 2(c) and oxidized to form a protective layer for the Al film; this controlled oxidation is preferred over natural oxidation of aluminum as a result of exposure to the oxygen in air. The purpose of the two slits in both the ground and capacitor electrodes, into which the two junction electrodes fit, is to avoid any discontinuity in the deposited electrodes due to shadowing. Having slits is not a general necessity; we added them to keep the electrodes and the wiring layout as close as possible to the design of our standard devices. Next, the surface is prepared for patching, i.e., removing the oxide atop the Al films in the fringes. This is achieved by Ar^+ ion milling of the substrate at $\theta = -45^\circ$ and $\varphi = 45^\circ$ [Fig. 2(d)]. At this angle, the resist wall protects the junction area from being milled away. Al is then deposited from the same angle in order to form the patch [Fig. 2(e)]. The Al is anew oxidized to create a protective oxide. Figure 2(f) shows a scanning electron micrograph (SEM) of the junction and the patch after liftoff. Note that the two electrode ends are slightly wider than the junction width itself, for better contact between the electrode and the fringes.

Apart from φ and θ , three other parameters have to be taken into account in this process:⁹ the resist thickness s , the width of a fringe f , and the width of the junction electrodes d . The cross-type technique requires that $s > d \tan \varphi$ to obtain selective electrode deposition²³ [3D schematic, Fig. 2(b)]. However, here the more stringent condition $s > d\sqrt{2} \tan \varphi$ applies to avoid deposition or milling of the junction area when forming the patch layer. Additionally, it is required that $f < s/(\sqrt{2} \tan \varphi)$ to avoid Al deposition on the fringes during deposition of the electrodes, assuming a fringe angle of 45° [3D schematic on Fig. 2(d)]. For all of these inequalities, φ is left variable. In our implementation, $s = 0.95 \mu\text{m}$, $f = 0.4 \mu\text{m}$, and $\varphi = 45^\circ$.

We note that other patch patterns exist, which can connect the junction electrodes to the rest of the circuit—the key is to shape them such that they are shadowed and protected from the evaporating metal when the junction is being made.

In order to quantitatively investigate the quality of the junctions made by the PICT process, we fabricated Xmon qubits and compared their performance against our benchmark.²⁸ Our study involves two chips designated as S (standard) and P (PICT), each containing three Xmons denoted X1, X2, and X3. To establish a fair comparison between the two processes, we fabricated both chips on the same wafer so that they would undergo the exact same steps for the ground plane and wiring layer until the wafer was split into two for the fabrication of the junctions and the patches. Each chip was packaged and wire bonded in a copper box, mounted onto the mixing chamber of a dilution refrigerator, and measured at a temperature below 12 mK.

TABLE I. Parameters of the measured qubits. For each qubit, the junction area is based on the design parameters, while the qubit frequency, f_{01} , the relaxation time, T_1 , and the free-induction decay time, T_2^* , were measured. Note that T_1 and T_2^* are shown as means, given in μs , plus/minus one standard deviation, given in percent, representing temporal fluctuations around the mean.²⁸

Qubit	Junction area (μm^2)	f_{01} (GHz)	T_1 (μs)	T_2^* (μs)	Q (10^6)
S-X1	0.024	4.219	$54 \pm 23\%$	$73 \pm 22\%$	1.4
P-X1	0.024	4.19	$59 \pm 12\%$	$65 \pm 26\%$	1.6
S-X2	0.0225	4.268	$55 \pm 23\%$	$53 \pm 36\%$	1.5
P-X2	0.0225	4.15	$56 \pm 23\%$	$57 \pm 29\%$	1.5
S-X3	0.021	3.956	$48 \pm 35\%$	$41 \pm 37\%$	1.2
P-X3	0.021	3.933	$69 \pm 20\%$	$43 \pm 28\%$	1.7

Table I presents the qubit parameters. We find that the frequency of each qubit on the P chip matches that of its pair on the S chip within a few tens of MHz, which indicates that the PICT process did not cause any large variations in the frequency. We measured T_1 and T_2^* for each of the six qubits more than 250 times over a time span of approximately 15 h in order to capture the statistics of the ubiquitous parameter fluctuations.²⁸ Figures 3(a) and 3(c) show examples of measurements (data points) and their fits (continuous line) on qubit P-X1. Figures 3(b) and 3(d) show histograms of T_1 and T_2^* for qubits S-X1 and P-X1, showing very similar values between the chips. For all the qubits, the values of T_1 and T_2^* and their standard deviations are summarized in Table I. Since these qubits have different frequencies, we can most fairly compare their performance by rescaling their T_1 to the quality factor Q . The average Q for the PICT-JJ qubits is 1.6×10^6 , while for the standard qubits, we obtain a negligibly different number: 1.4×10^6 .

We studied the reproducibility of the normal state resistance for junctions fabricated using the PICT process. The transmon qubit is essentially an anharmonic oscillator with fundamental transition frequency¹²

$$f_{01} \approx 1/(2\pi\sqrt{L_J C}) - E_C/h. \quad (1)$$

Here, the charging energy, $E_C = e^2/(2C)$, depends on the qubit's total capacitance C , where e is the electron charge. The Josephson inductance, $L_J = \Phi_0/(2\pi I_c)$, depends on the junction critical current, I_c . ($\Phi_0 = h/(2e)$ is the magnetic flux quantum and h is Planck's constant.) In turn, I_c is related to the junction normal-state resistance, R_N , via the Ambegaokar–Baratoff relation,²⁹ $I_c R_N = \pi\Delta/(2e)$. These equations indicate that C and R_N are the parameters that can influence the reproducibility of the qubit frequency across a wafer. The material and thickness-dependent gap parameter, Δ , is not expected to fluctuate across a wafer at zero temperature.^{31–33} The capacitance C is dominated by a large planar capacitor with small fabrication-induced variation. Simulation shows that even $0.3 \mu\text{m}$ variation in the linewidth of the capacitor changes the capacitance by $\sim 1\%$. As a result, R_N is the dominant parameter that causes variation in the qubit frequency, and following the analysis of Ref. 6, the deviation in f_{01} is half that of R_N .

Statistical studies of normal resistance have been reported for both niobium- and aluminum-based JJs fabricated using different methods. Table II summarizes these studies, the most recent of which

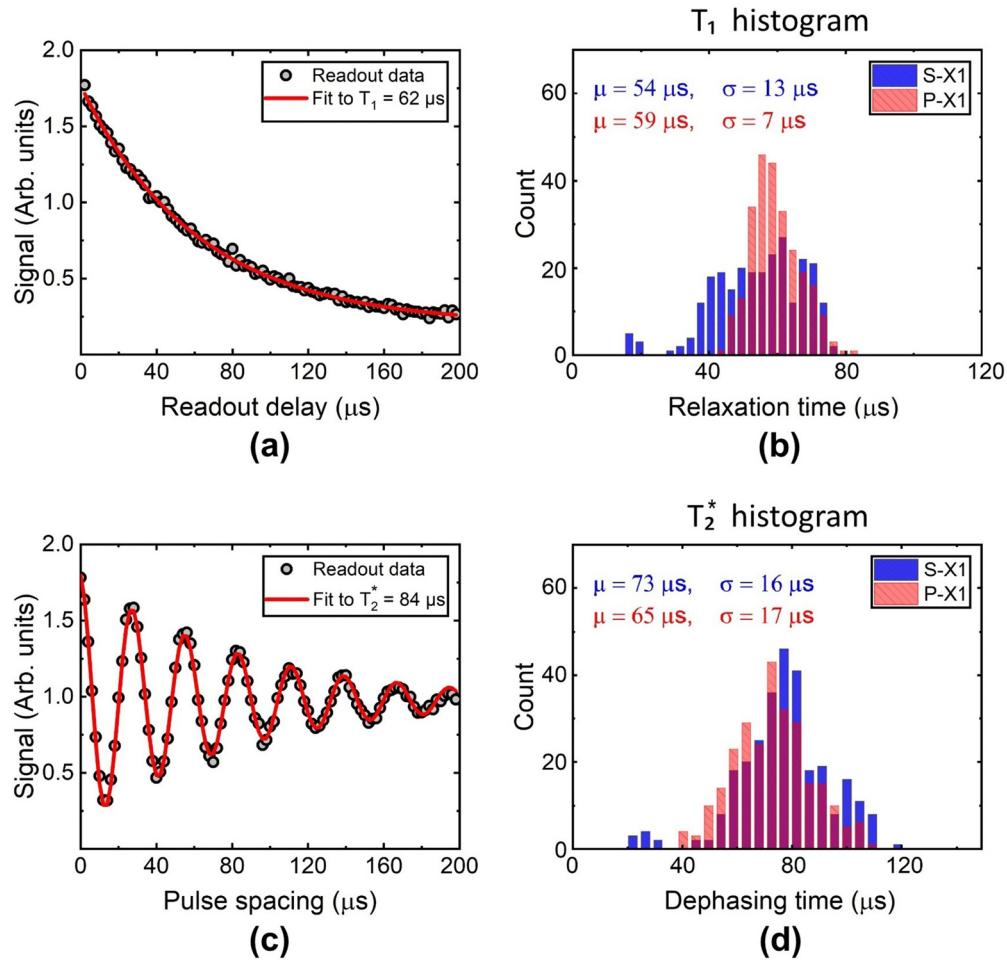


FIG. 3. Coherence characterization for two different qubits, S-X1 (standard process) and P-X1 (PICT process). (a) and (c) represent T_1 and T_2^* data and fits for one measurement iteration on P-X1. (b) and (d) are histograms of T_1 and T_2^* over 250 measurements on both S-X1 and P-X1.

is a larger-scale reproducibility study over several wafers by Kreikebaum *et al.*¹⁰ They showed an average on-chip variation of 1.8% and a wafer-scale spread of less than 3.5% although during subsequent fabrication of qubits, it increased to 6.9%.

Using the PICT process, we fabricated thousands of test junctions and measured their resistance for a wafer-scale study of reproducibility.

The 76-mm wafer included forty chips of size $0.5 \times 0.5 \text{ cm}^2$, and each chip had 100 test junctions with 10 different sizes. The focus of this study was on small JJs (0.01 to $0.16 \mu\text{m}^2$), the typical sizes used for transmon qubits. We measured the junction resistances using an automated probe station at room temperature (only measurements with a coefficient of determination higher than 0.99 were considered).

TABLE II. Statistical studies of the normal resistance of niobium and aluminum-based Josephson junctions, both with an aluminum-oxide tunnel barrier.

References	Material	JJ area (μm^2)	Variation (%) wafer-level	Variation (%) chip-level
Bumble <i>et al.</i> ⁵	Nb	0.33	...	2–4
Tolpygo <i>et al.</i> ⁸	Nb	0.03–1.8	0.8–8	...
Lotkhov <i>et al.</i> ⁴	Al	0.125–0.25	10–20	...
Pop <i>et al.</i> ⁷	Al	0.02–0.2	...	3.5
Kreikebaum <i>et al.</i> ¹⁰	Al	0.042	3.5	1.8
This work	Al	0.01–0.16	2.5–6.3	1.2–2.9

Figure 4(a) shows a heat map of the fabrication yield of each chip. The total wafer-scale yield is about 99.1%. The bottom panel of Fig. 4(b) shows the yield as a function of junction size over the whole wafer.

The top panel of Fig. 4(b) shows the mean resistance for each junction size across the wafer, $\overline{R_N}(A)$, on a log scale with error bars representing one standard deviation. The continuous line is a linear fit with a slope of ~ -0.9 , close to the expected number of -1 , since $R_N \propto 1/A$. The deviation from the -1 slope is caused by the constant linewidth bias (here ~ 28 nm) in the EBL pattern compared to the computer-aided design (CAD). A heat map for the average normalized resistance, $\overline{R_0}$, of each chip is shown in Fig. 4(c). To obtain R_0 for one junction, its resistance is divided by the mean resistance of junctions with the same size across the wafer, such that $R_0 = R_N/\overline{R_N}$. The observed gradient of $\overline{R_0}$ over the wafer may be caused by uneven development and desumming (oxygen plasma).

The inter-chip variation of the resistance is 3.7% across the wafer, and the average on-chip spread is 2.7%, with three chips having a spread as low as 1.4%. The variation of R_N has a strong size dependence,⁸ especially for small junctions, as shown in Fig. 4(d). The figure compares histograms of R_0 for four different junction areas across the wafer. Figure 4(e) shows, in red squares, the coefficient of variation (CV) of R_N as a function of the junction area for all junction sizes.

Variation in R_N is caused by fluctuations in both the junction area A and the tunnel barrier thickness, which corresponds to a critical-current density, J_c . For the latter, we use the Ambegaokar–Baratoff relation²⁹ and write $R_J = \pi\Delta/(2eJ_c)$ (with units Ωm^2), and we obtain

$$R_N = \frac{R_J}{A}. \quad (2)$$

Parenthetically, we disregard any contribution to the fluctuation of the measured normal-state resistance from electrode thickness variations across the wafer (in series with the junctions), which we estimate to be $<0.5\%$. Assuming R_J and A are independent variables, the CV of R_N can be expressed as^{34,35}

$$(CV_{R_N})^2 = (CV_{R_J})^2(CV_A)^2 + (CV_{R_J})^2 + (CV_A)^2. \quad (3)$$

In this equation, CV_{R_J} is solely determined by the uniformity of the oxide barrier across the wafer. On the other hand, we can derive an expression for CV_A in terms of A itself. Given the simple case of a square junction with side length d , $A = d^2$ and $\sigma_A = 2d\sigma_d$, where σ denotes the standard deviation. Dividing the latter equation by A , we obtain $CV_A = \sigma_A/A = 2\sigma_d/\sqrt{A}$. Now, σ_d is mainly determined by the lithography process, including exposure, development, and desumming, and it is assumed to be a certain constant that does not scale with d . One can then fit the data in Fig. 4(e) to Eq. (3) after substituting for CV_A and extract the constants CV_{R_J} and σ_d from the fit. We find $CV_{R_J} = 2.3\%$ and $\sigma_d = 3$ nm. CV_A as a function of the junction area is plotted in Fig. 4(f). This determination of CV_A and σ_d was done using the nominal, designed junction area; however, we can improve the accuracy by taking into account the previously determined 28 nm linewidth bias. In this way, we find $CV_{R_J} = 1.8\%$ and $\sigma_d = 4$ nm. For the typical JJ sizes (0.02 – $0.06\ \mu\text{m}^2$) used for

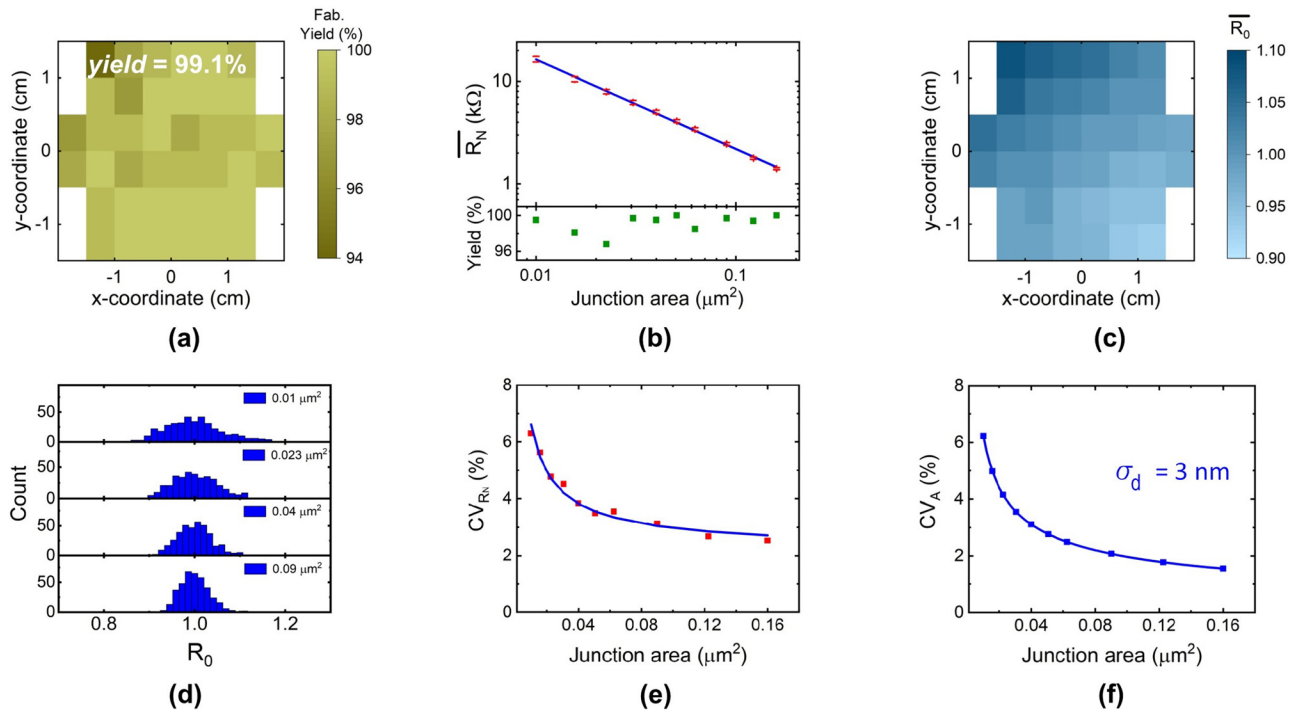


FIG. 4. Reproducibility of the PICT junction resistance. (a) Heat map of the fabrication yield for forty $5 \times 5\text{-mm}^2$ chips across a 76-mm wafer. (b, top) Mean value of R_N , with error bars (red), vs junction area, and a linear fit (blue). (b, bottom) Fabrication yield vs junction area. (c) Heat map of the average normalized resistance, $\overline{R_0}$. (d) Histograms of R_0 for four different junction areas. (e) CV_{R_N} (points) vs junction area and a decaying fit (continuous line) to Eq. (3). (f) CV_A vs junction area, according to the equation $CV_A = 2\sigma_d/\sqrt{A}$.

fixed-frequency transmon qubits, $\sigma_d = 4$ nm corresponds to CV_A of 2.9%–4.6%, that is, 60%–70% of the total variation in R_N is attributed to fluctuations in the junction area, while the rest is attributed to the inhomogeneity of the tunnel barrier.

Improving the reproducibility of R_N requires minimizing the two parameters CV_{R_j} and σ_d . For CV_{R_j} , it was shown that the uniformity of the AlO_x barrier heavily relies on the uniformity and the morphology of the underlying Al layer in addition to the oxidation conditions.³⁶ For σ_d , the lithographic process is the main contributor. A high-resolution resist and an optimized EBL process, in addition to an improved recipe of resist development and descumming, can lead to a minimal deviation in the feature size.^{10,37}

To summarize, we proposed and demonstrated a simplified process to fabricate a Josephson junction and its patch layer that provides a superconducting, galvanic connection of the junction to the circuit. The process relies on shadow evaporation from three angles and fabricates the junction and the patch in only one lithography step. Suitable for making superconducting qubits, our method reduces the total number of junction fabrication steps by half without introducing further losses. Moreover, we statistically studied the reproducibility of the junctions and achieved a high fabrication yield. The junctions' resistance variation showed a strong dependence on the width, with an average variation of less than 3.7%, comparable to the best values that are reported by other research groups. The variation can be reduced by optimizing the lithography process and by improving the uniformity of the tunnel barrier.

Note added. A related JJ-fabrication technique, named the *in situ* bandaged junction (ISBJ), was recently and independently developed by Bilmes *et al.*³⁸

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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